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Remarks

Claims 1-2, 4-19, 21-37 and 39-40 are pending in the application. Claims 1 and 18 have been amended to include the subject matter of original claims 17 and 34, respectively, and claims 17 and 34 have been canceled. Claim 35 has been amended to depend from amended claim 18. Favorable reconsideration of the application, as amended, is respectfully requested.

I. REJECTION OF CLAIMS UNDER 35 USC §102

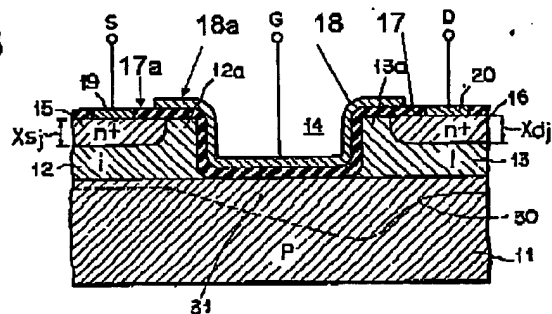
Claims 1, 4, 7, 12, 13, 15, 17, 18, 21, 25, 29-31, 34, and 39 stand rejected under 35 USC §102(b) as being anticipated by *Natori* (U.S. 4,243,997). Claims 1, 2, 4, 7, 13, 15, 18, 19, 21, 25, 30 and 31 stand rejected under 35 USC §102(e) as being anticipated by *Liu* (U.S. 6,528,847).

Claims 1 and 18 have been amended to include the subject matter of original claims 17 and 34, respectively, and now recite a memory cell having a control gate formed over the gate dielectric layer, wherein an upper surface of the control gate is substantially at the same level as an upper surface of the gate dielectric layer.

The Examiner rejected original claims 17 and 34 under 35 USC §102(b) based on *Natori*. The Applicant respectfully disagrees with the Examiner's rejections for at least the following reasons.

In rejecting original claims 17 and 34 (now amended claims 1 and 18) based on *Natori*, the Examiner cites to Fig. 3 of *Natori* (reproduced at right), and states the upper surface of the gate is "substantially" at the same level as the upper surface of the gate dielectric layer. Figure 3 of *Natori* illustrates a gate electrode 18 formed over a dielectric layer 17. As can be seen in Fig. 3, an upper surface 18a of the gate electrode 18 is above an upper surface 17a of the dielectric layer 17 by the

FIG. 3



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thickness of the gate electrode.¹ While *Natori* does not explicitly disclose the thickness of the gate electrode 18, a gate electrode typically has a thickness on the order of about 100 to 400 nm. Using this range, the upper surface 18a of the gate electrode 18 is 100 to 400 nm above the upper surface 17a of the dielectric layer 17.

Admittedly, a thickness of 100 to 400 nm is small in the context of many applications. In the field of semiconductor devices, however, such a thickness is considered significant. Clearly, *Natori* does not teach or suggest that an upper surface of the control gate is substantially at the same level as an upper surface of the gate dielectric layer, as recited in amended claims 1 and 18.

Liu discloses a semiconductor device wherein a control gate is formed over the gate dielectric layer.² Thus, *Liu* does not make up for the deficiencies of *Natori*.

Accordingly, withdrawal of the rejection based on *Natori* and *Liu* is respectfully requested.

II. REJECTION OF CLAIMS UNDER 35 USC §103

Claims 1, 2, 4, 7-10, 12, 13, 17-19, 21, 25-27, 29, 30, 34, 39 and 40 stand rejected under 35 USC §103(a) as being unpatentable over *Willer* (U.S. 6,661,053). Claims 5, 6, 11, 14-16, 22-24, 28, 31-33, 36 and 37 stand rejected under 35 USC §103(a) as being unpatentable over *Willer* in view of *Palm et al.* (U.S. 2002/0024092). Claim 35 stands rejected under 35 USC §103(a) as being unpatentable over *Willer* in view of *Wollesen* (U.S. 5,960,271).

As was noted above, claims 1 and 18 have been amended to include the subject matter of original claims 17 and 34. While the Examiner rejects original claims 17 and 34 as being unpatentable over *Willer*, the Examiner, other than making the rejection, does not address the rejection in the Office Action. Applicant has reviewed the figures of *Willer* and in each of the embodiments the gate electrode 4 is formed over the dielectric layer 9. Thus, an upper surface of the gate electrode is not at substantially the same level as an upper surface of the dielectric layer. *Willer* has not been found to

¹ Reference indicators 17, 17a, 18 and 18a were added to Fig. 3.

² See, e.g., column 7, lines 32-41 and Fig. 1E of *Liu*

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teach or suggest that an upper surface of the control gate is substantially at the same level as an upper surface of the gate dielectric layer, as recited in amended claims 1 and 18.

Accordingly, withdrawal of the rejection of amended claims 1 and 18 is respectfully requested.

Claims 2, 4-16, 19, 21-33, 35-37 and 39-40 directly or indirectly depend from either claim 1 or claim 18 and, thus, can be distinguished from the cited art for at least the same reasons.

Further, the Examiner contends original claim 35 is unpatentable over *Willer* in view of *Wollesen* (U.S. 5,960,271). Applicant respectfully submits that one skilled in the art would not be motivated to combine *Willer* and *Wollesen* for at least the following reasons.

Willer pertains to a memory cell wherein erase times are reduced compared to the prior art. Of primary importance in the memory cell of *Willer* is the curvature of the trench bottom. The curvature of the trench bottom and lower regions of the trench walls determine a field component which is aligned tangential to the trench wall. The lateral curve is situated between the actual bottom and the essentially vertical lateral wall of the trench in the region in which hole injection takes place.³

Wollesen pertains to a field effect transistor (FET) that provides for a short channel length that can be formed using conventional (pre 1998) lithography to define gate lengths much shorter than the lithographic limit. To obtain such results, *Wollesen* describes a transistor having a V-shape trench with an angle of about 57 degrees relative to a surface of the silicon body.⁴ The V-shape trench (and gate electrode residing therein) cause the effective channel length to extend along the source side of the trench, while large depletion regions form on the drain side of the trench.⁵ The major advantage of this V-shape gate electrode is that a gate width can be

³ Column 4, lines 44-56 of *Willer*

⁴ Column 4, lines 37-39 of *Wollesen*

⁵ Column 6, lines 58-64 and Figs. 17a and 17b of *Wollesen*

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lithographically formed more than two and up to five times larger than the desired effective channel length.⁶

Accordingly, important features of both *Willer* and *Wollesen* are the respective shapes of the trenches. *Willer* requires a trench having a curvature along the bottom and at the side walls, while *Wollesen* requires a trench having a V-shape. Combining the teachings of *Willer* and *Wollesen* destroys the primary inventive aspect of each invention. Thus, one skilled in the art would not be motivated to combine *Willer* and *Wollesen*. *Palm et al.* has not been found to make up for the deficiencies of *Willer* and *Wollesen*.

Accordingly, withdrawal of the rejection of claims 2, 4-16, 19, 21-33, 35-37 and 39-40 is respectfully requested.

III. CONCLUSION

Accordingly, all pending claims are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

⁶ Column 7, lines 8-12 of *Wollesen*

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Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

In the event any fee or additional fee is due in connection with the filing of this paper, the Commissioner is authorized to charge those fees to our Deposit Account No. 18-0988 (under the above Docket Number). In the event an extension of time is needed to make the filing of this paper timely and no separate petition is attached, please consider this a petition for the requisite extension and charge the fee to our Deposit Account No. 18-0988 (under the above Docket Number).

Respectfully submitted,

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